REMARKS

By this amendment, new claims 58-63 have been added. Claims 1-6 and 58-63 are pending in the application. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Claims 1-6 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation of "a location outside of a production facility of said die" derives support from paragraphs [0086]-[0089] of the specification, which describe exemplary embodiments in which the invention is used "in the field" and is tested and repaired after leaving the production facility. Applicant respectfully requests that the rejection of these claims be withdrawn.

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Brauch et al. (US 6,550,023) in view of Wada et al. (US 6,138,257). This rejection is respectfully traversed. In order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. §2142. Neither Brauch et al. nor Wada et al., even when considered in combination, teach or suggest all limitations of independent claim 1.

Claim 1 recites, *inter alia,* a method of testing a memory die, comprising "allowing said memory die to be placed in a location outside of a production facility of said die; [and] testing said memory die while said die is in said location" (emphasis added). Wada et al. does not teach or suggest this limitation. Wada et al. teaches that "it is absolutely necessary to inspect electrical characteristics of all or some of the IC devices at individual stages of manufacturing and testing stations." Col. 1, ln. 12-15 (emphasis added). There is no location outside of a production facility as recited in

claim 1. Nor is Brauch et al. cited for this limitation. Thus, Brauch et al. does not remedy the deficiency of Wada et al.

Further, "as a 'useful general rule,' . . . references that teach away [from a particular combination] cannot serve to create a prima facie case of obviousness." *McGinley*, 262 F.3d at 1353-4, citing *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994). Wada et al., in fact, teaches away from the claimed limitation as defined in the Office Action, teaching "[i]n some cases, ... defect analysis test is performed off the mass production line extractively for selected ones of the manufactured ICs rather than on the mass production line for every manufactured IC, but such an extractive defect analysis test is not desirable from a viewpoint of quality control. [I]t is preferred to perform the defect analysis test for every manufactured IC, which would ... present the problem that a longer test time is required." Col. 2, ln. 41-49 (emphasis added).

Since Brauch et al. and Wada et al. do not teach or suggest all of the limitations of claim 1, claim 1 and dependent claims 2-6 are not obvious over the cited references. Applicant respectfully requests that the 35 U.S.C. § 103(a) rejection of claims 1-6 be withdrawn.

Claims 58-60 contain the same subject matter as previously cancelled claims 10-12. Claims 61-63 contain the same subject matter as previously cancelled claims 55-57. Claims 10-12 and 55-57 were rejected in an Office Action dated April 8, 2005 under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto et al. (US 6,246,618). Claims 58, 61, and 63 recite, *inter alia*, a method of processing a plurality of memory circuits comprising "incorporating said plurality of memory circuits into an electronic system, said system having a primary function other than test or repair of said plurality of memory circuits" (emphasis added). Yamamoto et al. does not teach or suggest this limitation. Yamamoto et al. teaches that "[t]he scan control extracts a signal for test ...

from an outside apparatus for generating a signal for test.... The control signal for scan test is output to the RAMs 10 to 13.... Output signals (memory output signals) are extracted from the RAMs 10 to 13 ... and the memory output signal from one of the RAMs is output to an outside test apparatus." Col. 8, ln. 63-Col. 9, ln. 2 (emphasis added). The memory circuits are not incorporated into a system having a primary function other than test or repair as recited in claim 1. Thus, the assertion in the Office Action does not remedy the deficiency of Yamamoto et al. Since Yamamoto et al. does not teach or suggest all of the limitations of claims 58, 61, and 63, claims 58, 61, and 63 are not obvious over the cited reference. Claims 59-60 depend from claim 58 and are patentable at least for the reasons mentioned above. Claim 62 depends from claim 61 and is patentable at least for the reasons mentioned above.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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